REMARKS

The Examiner's Action dated August 26, 1992, has been received, and its contents carefully noted. In addition, receipt is acknowledged, with appreciation, of the Examiner Interview Summary Record dated September 15, 1992, in which the Examiner confirms that the office action of August 26, 1992 does not present a final rejection.

In order to advance prosecution, the previously pending claims have been cancelled and replaced by new method claims 25-28. These claims have been drafted to define the contribution of the invention over the prior art with greater particularity.

Claim 25 distinguishes over the prior art in that it specifies that both the lower conductor structure and the upper conductor structure is formed from at least one layer and a metal plating layer which is formed on, and adheres to, the at least one layer. By this method, the advantages offered by the conductor structure fabrication method according to the invention, relating particularly to elimination of stress migration and electro migration, as well as voids and projections in the conductor structures, can be fully realized. It will be noted that in the method defined in claim 25 the lower conductor structure, which is covered with an insulating layer, is formed in the manner described above. One significant result is that projections, such as shown at 1116 in Fig. 2(b) will not grow on the lower conductor structure during subsequent heating processes. These projections promote current leakage between insulating layers. Specification, page 5, lines 1-4.

In the method described at column 10, lines 13-65 of Del Monte, a contact electrode bump 23 is formed by electroplating. It also appears possible that a gold flash layer 21 is formed by electroplating. However, this is not completely certain since the cited portion of the reference specification states that "a very

thin gold flash layer is sputtered on the entire surface of the wafer." Lines 9-10. It is well recognized in the art that sputtering is a process which is quite different from electroplating. In any event, this reference only discloses plating associated with forming an electrode bump and there is no disclosure of forming an insulating layer over a plated layer or of subsequently subjecting the device to a heat treatment which would result in the creation of projections. In more general terms, there is no disclosure in this reference that any advantage would be served by forming conductor structures with a plating layer when those conductor structures are at least partially separated by an insulating layer.

In further accordance with the disclosure of this reference, the layer on which the layer 17-23 is formed is identified simply as an interconnection network made of aluminum. Column 6, lines 32-39. There is nothing in the disclosure of this reference which would suggest to one skilled in the art any particular method for fabricating the interconnection network 11.

The primary reference, McDavid, does not disclose a device including a lower conductor structure and an upper conductor structure, with the upper conductor structure being connected to the lower conductor structure.

Thus, no reasonable combination of the teachings of the applied references can be considered to suggest the method now defined in claim 25.

Claim 26 further defines patentably over the applied references by its recitation that the at least one layer of the upper conductor structure contact the metal plating layer of the lower conductor structure.

Claim 27 defines patentably over the prior art by its recitation that the step of forming an upper conductor structure includes, after the plating operation, performing a thermal

treatment in order to diffuse material from the plating layer into the at least one layer. Such a step is not disclosed in either of the applied references. As described at page 12, lines 11-15 of the present specification, the plating operation in combination with the thermal treatment results in a device in which the projections 1116 depicted in Figures 1 and 2 are entirely avoided.

Claim 28 is directed to a novel embodiment of the invention, one example of which is illustrated in Figures 5d and e of the application drawing, according to which the metal plating layer is deposited in openings formed in a patterned resist layer, after which the resist layer is removed and portions of the conductor layer underlying the plating layer are removed by etching, using the plating layer as a mask. This method is described in the specification, particularly at page 16. This represents an efficient method for giving the conductor structure a well defined configuration. A particular advantage is that the plating layer performs the dual function of improving the performance characteristics of the conductor structure and serving as an etching mask. The outline of the resulting conductor structure is well defined in view of the inherent ability of plating to form a uniform layer which completely fills an opening in a plating mask.

The method defined in claim 28 is not disclosed in or suggested by the applied references.

Accordingly, it is believed that the claims now in the application define methods which bear no relation to those disclosed in the applied references, and therefore define patentably thereover. It is therefore requested that the rejections of record be reconsidered and withdrawn and that the application be allowed.

If for any reason, the Examiner finds the application in other than a condition for allowance, he is respectfully requested to call the undersigned attorney at the Washington, D.C. telephone number 223-5700 to discuss the steps necessary for placing the application in condition for allowance.

11/25/92
Date

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to the Commissioner of Patents and Trademarks, Washington, D.C. 20231 on November 25, 1992.

Jay M. Finkelstein, Reg. No. 21,082

(signature) (date) 11/25/92